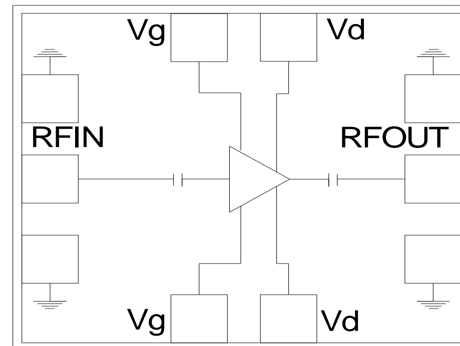
7.3 – 9.6 GHz 4 Watt Power Amplifier

Features

- **Frequency Range : 7.3 – 9.5GHz**
- **36 dBm output P1dB**
- **8 dB Power gain**
- **28% PAE**
- **High IP3**
- **Input Return Loss > 8 dB**
- **Output Return Loss > 10 dB**
- **Dual bias operation**
- **No external matching required**
- **DC decoupled input and output**
- **0.5 µm InGaAs pHEMT Technology**
- **Chip dimension: 2.5 x 2.8 x 0.1 mm**

Functional Diagram



Typical Applications

- **RADAR**
- **Military & space**
- **LMDS, VSAT**

Description

The ASL4012 is a X-band power amplifier with 36dBm power output. The PA operates in 7.3 – 9.6 GHz frequency range. The PA features 8 dB of gain with input and output return losses of 8 dB and 10 dB respectively. The PA has a high IP3 of 44dBm and 28% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage. The die is fabricated using a reliable 0.5µm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings [1]

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+10	volts
Drain current (Id)	1.6	A
RF input power (RFin at Vd=9V)	35	dBm
Operating temperature	-50 to +85	ºC
Storage Temperature	-65 to +150	ºC

1. Operation beyond these limits may cause permanent damage to the component

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Electrical Specifications [(1)] @ T_B = 40 °C, V_d =8V, V_g =-0.9V, Z_o =50Ω

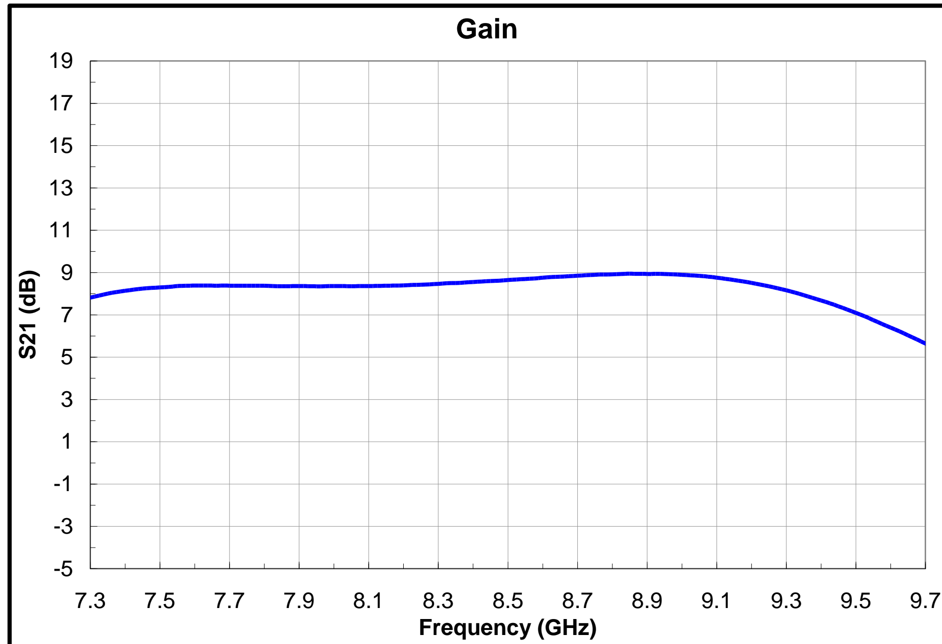
Parameter	Min.	Typ.	Max.	Units
Frequency	7.3		9.6	GHz
Small Signal Gain	-	8	-	dB
Gain Flatness	-	± 0.5	-	dB
Input Return Loss	-	8	-	dB
Output Return Loss	-	10	-	dB
Output 1dB Compression Point (P1dB)	-	+36	-	dBm
Output 3rd Order intercept Point (IIP3)[1]	-	44	-	dBm
PAE [2]	-	28	-	%
Drain Bias Voltage (Vd)	-	+8	+9	V
Gate Bias Voltage (Vg)	-1.0	-0.9	-0.8	V
Supply Current (Idq)	-	1.3	-	A
Supply Current (Idsat)		1.6		A

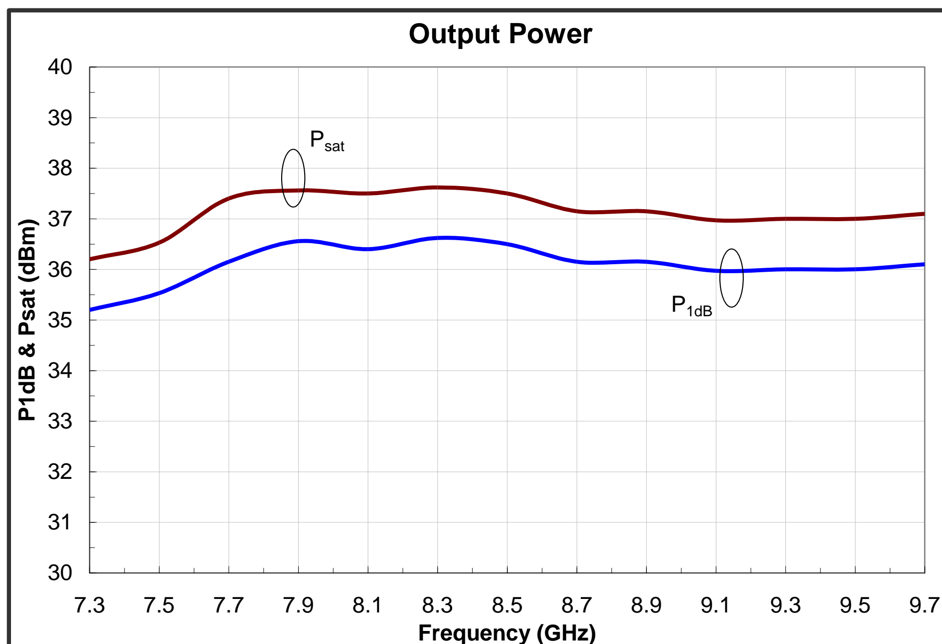
Note:

1. T_B – MMIC base temperature
2. Measured at output 1dB compression point
3. Operaing current should be present in between Idq and Idsat.

Test fixture data

T_B=40^{0}C, Z_0 = 50Ω, Vd = 8V, Idq = 1.3A





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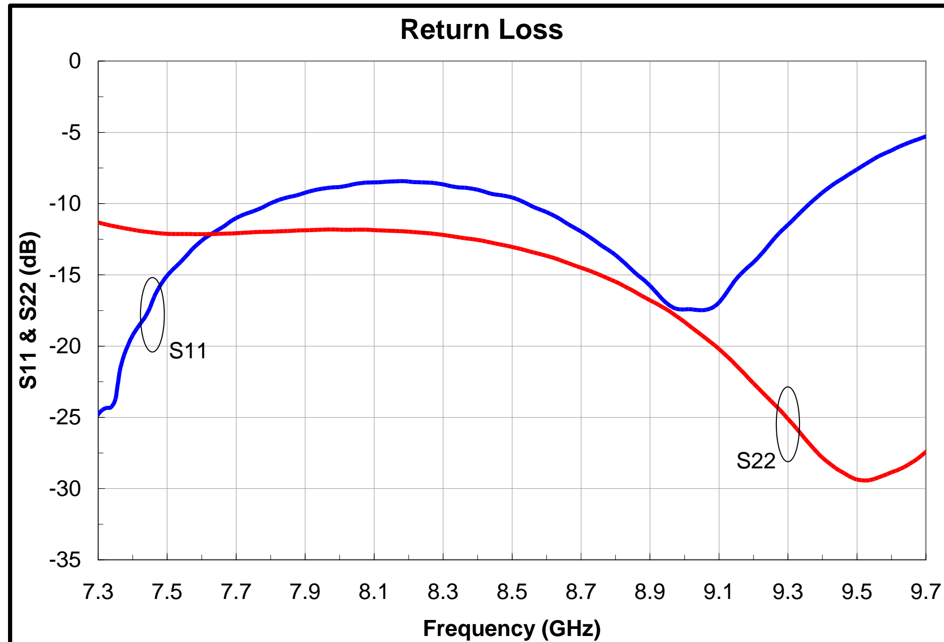
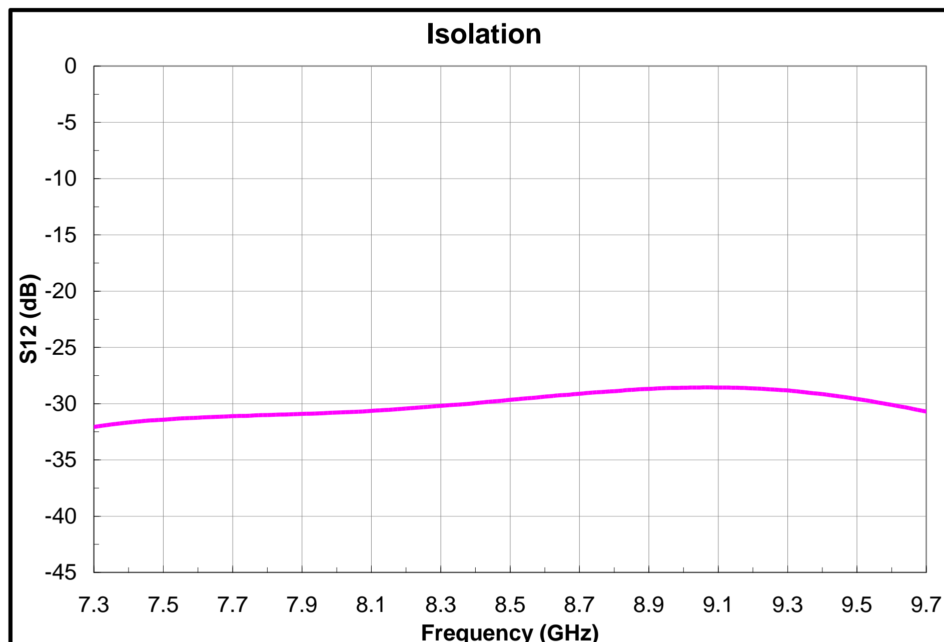
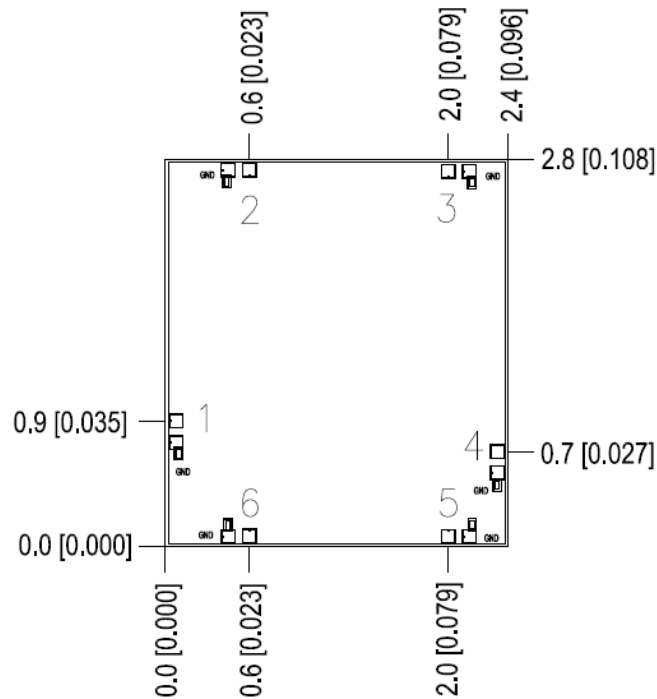




Bond Pad Locations



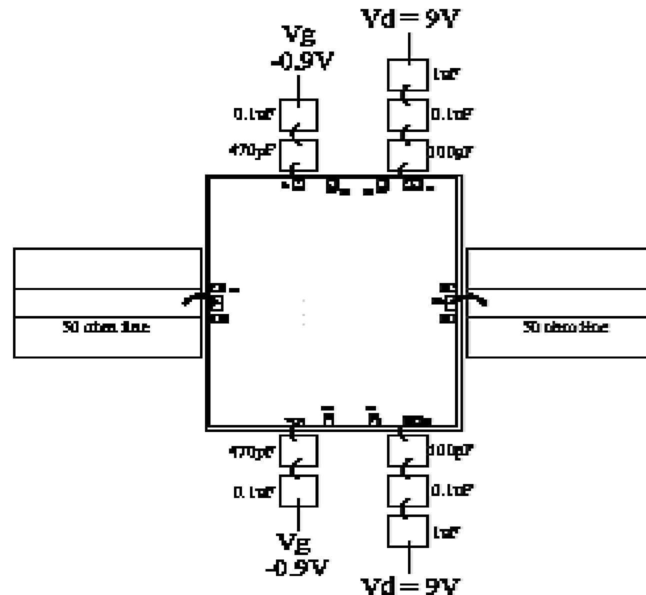
Units: millimeters [Inches]

Note:

1. All RF and DC bond pads are 100µm x 100µm
2. Pad no. 1 : RF IN
3. Pad no. 3,5 : Drain voltage(V_d)
4. Pad no. 4 : RF Output
5. Pad no. 2,6 : Gate voltage (V_g)

Note: All RF and DC bond pads are 100µm x 100µm unless specified

Recommended Assembly Diagram



Note:

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF capacitor.
3. Input and output 50 ohm lines are on 5 mil RT Duroid substrate
4. 0.1 μF capacitors may be additionally used as a second level of bypass for reliable operation
5. The RF input & output ports are DC decoupled on-chip.
6. Proper heat sink like Copper tungsten or copper molybdenum to be used for better reliability of chip

Die attach: For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200μm length of wedge bonds is advised. Single Ball bonds of 250-300μm though acceptable, may cause a deviation in RF performance.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice

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